

# Voltage Sag Compensation of Point of Common Coupling (PCC) Using Fault Current Limiter

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**Abstract**—In this paper, voltage sag compensation of point of common coupling (PCC) using a new structure of fault current limiter (FCL) is proposed. The proposed structure prevents voltage sag and phase angle jump of substation PCC after fault occurrence. This structure has a simple control method. Using semiconductor switch (IGBT or GTO) at dc current rout leads to fast operation of the proposed FCL and consequently, dc reactor value is reduced. On the other hand, the proposed structure reduces total harmonic distortion (THD) on load voltage and it has low ac losses in the normal operation. As a result, other feeders which are connected to the substation PCC will have good power quality. Analytical analysis, simulation results using PSCAD/EMTDC software and experimental results are presented to validate effectiveness of this structure.

**Index Terms**—Voltage sag, fault current limiter, power quality, point of common coupling (PCC), semiconductor switch, THD.

## I. INTRODUCTION

Electric power quality can be defined as the capacity of an electric power system to supply electric energy of a load in an acceptable quality. Many problems can result from poor power quality, especially in today's complex power systems, such as false operation of modern control systems. Voltage sag is an important power quality problem because of sensitive loads growth. Worldwide experience shows that short circuit faults are the main origin of voltage sags and therefore the loss of voltage quality. This problem appears especially in buses which are connected to radial feeders [1-6].

The most common compensator for voltage sag is dynamic voltage restorer (DVR). The basic operation of the DVR is based on injection a compensation voltage with required magnitude, phase angle and frequency in series with sensitive electric distribution feeder [7, 8].

The voltage sag during the fault is proportional to the short circuit current value. An effective approach to prevent expected voltage sag and improve the voltage quality of point of common coupling (PCC) is fault current limitation by means of a device connected at the beginning of most exposed radial feeders [9].

Superconducting fault current limiter (SFCL) structures have proper characteristics to control the fault current levels due to their variable impedance in the normal and fault conditions [10-13]. However, because of high technology and cost of superconductors, these devices are not commercially available. Therefore, by replacing the superconducting coil with non-superconducting one in the FCL, it is possible to make it simpler and much cheaper. It is important to note that, the main drawback of non-superconductor is a power loss which is

negligible in comparison with the total power, provided by distribution feeder [14, 15].

The other structures which are introduced in [4, 16, 17], have two numbers of thyristor switches in AC branch of diode bridge. When the fault occurs, after fault detection, thyristor switch turns off at first zero crossing and the fault current is limited to an acceptable value. These structures have switching power loss and complicated control circuit because of thyristor switching in the normal operation. In addition, we know that thyristor operation delay (turn off at first zero crossing) makes interruption on structure performance. So, to limit the fault current between fault occurrence instant and thyristors turn off instant, a large reactor in dc route is used. Because of voltage drop, harmonic distortion and power losses, this large value of dc reactor is unfavorable.

In this paper a new topology of FCL is proposed for the voltage sag and the phase angle jump mitigation of the substation PCC. In section II, analytical analysis of voltage sag and phase angle jump is discussed. Then, in section III, the proposed FCL topology is introduced and its operation in a simplified power system is explained. In section V, the PSCAD/EMTDC software is applied to investigate the operational behavior of the proposed FCL in this power system and simulation results are analyzed. Experimental results are presented and adapted with the simulations in section VI.

## II. VOLTAGE SAG STUDY IN SIMPLIFIED POWER SYSTEM

Fig. 1 shows single line diagram of the power system. This figure shows a substation with only two feeders F1 and F2. However, the presented analysis can be extended to any number of feeders, easily. The F1 supplies a sensitive load. With a fault in the F2, the voltage sag occurs in the substation PCC.

Positive sequence equivalent circuit of such a system is shown in Fig. 2. To calculate the voltage sag, the simple voltage divider method is introduced in [18].

In the normal state, the voltage magnitude and its phase angle in the substation PCC can be expressed as follows:

$$\bar{V}_{PCC(N)} = \frac{\bar{Z}_{K(N)}}{(\bar{Z}_S + \bar{Z}_I) + \bar{Z}_{K(N)}} \bar{V}_s \quad (1)$$

$$V_{PCC(N)} = \left| \frac{\bar{Z}_{K(N)}}{(\bar{Z}_S + \bar{Z}_I) + \bar{Z}_{K(N)}} \right| |\bar{V}_s| \quad (2)$$

$$\phi_{PCC(N)} = \arctan\left(\frac{X_{K(N)}}{R_{K(N)}}\right) - \arctan\left(\frac{X_{K(N)} + X_S + X_I}{R_{K(N)} + R_S + R_I}\right) \quad (3)$$

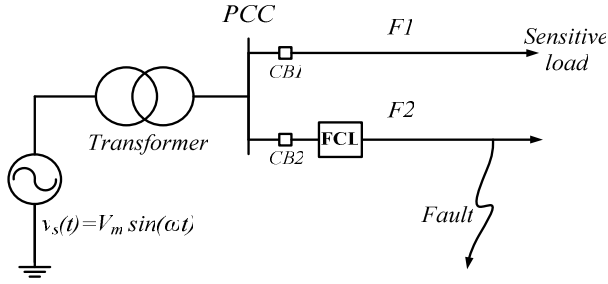


Fig. 1. Single line diagram of power system

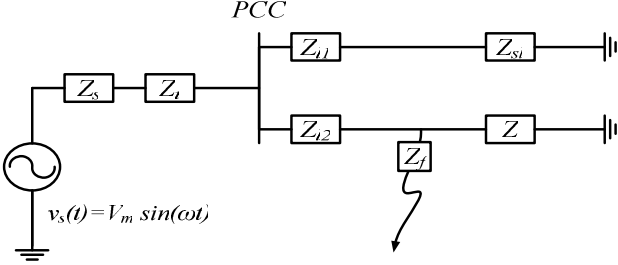


Fig. 2. Positive sequence equivalent circuit of the case study system in the fault condition

where:

$\bar{V}_{PCC(N)}$ : Voltage phasor of PCC in the normal state;

$V_{PCC(N)}$ : Voltage magnitude of PCC in the normal state;

$\phi_{PCC(N)}$ : Phase angle of PCC voltage in the normal state

where, the phase angle of  $\bar{V}_s$  is considered to be zero;

$\bar{Z}_t$ : Phasor of transformer impedance;

$\bar{Z}_s = R_s + jX_s$ : Phasor of source impedance;

$\bar{V}_s$ : Phasor of source voltage;

$\bar{Z}_{K(N)} = R_{K(N)} + jX_{K(N)}$ : Equivalent impedance of parallel feeders in the normal condition, i.e.:

$$\bar{Z}_{K(N)} = (\bar{Z}_{L1} + \bar{Z}_{SL}) \parallel (\bar{Z}_{L2} + \bar{Z}) \quad (4)$$

$\bar{Z}$ : Phasor of load impedance at the F2.

In the normal state,  $|\bar{Z}_{K(N)}|$  is greater than  $|\bar{Z}_s + \bar{Z}_t|$ . So, the PCC voltage is almost equal to the source voltage.

In the fault condition in the F2, the voltage and phase angle of substation PCC can be expressed as follows:

$$\bar{V}_{PCC(F)} = \frac{\bar{Z}_{K(F)}}{(\bar{Z}_s + \bar{Z}_t) + \bar{Z}_{K(F)}} \bar{V}_s \quad (5)$$

$$V_{PCC(F)} = \left| \frac{\bar{Z}_{K(F)}}{(\bar{Z}_s + \bar{Z}_t) + \bar{Z}_{K(F)}} \right| |\bar{V}_s| \quad (6)$$

$$\phi_{PCC(F)} = \arctan\left(\frac{X_{K(F)}}{R_{K(F)}}\right) - \arctan\left(\frac{X_{K(F)} + X_s + X_t}{R_{K(F)} + R_s + R_t}\right) \quad (7)$$

where:

$\bar{V}_{PCC(F)}$ : Voltage phasor of PCC during fault;

$V_{PCC(F)}$ : Voltage magnitude of PCC during fault;

$\phi_{PCC(F)}$ : Phase angle of voltage of PCC during fault;

$\bar{Z}_{K(F)} = R_{K(F)} + jX_{K(F)}$ : Equivalent impedance of parallel feeders during fault, i.e.:

$$\bar{Z}_{K(F)} = (\bar{Z}_{L1} + \bar{Z}_{SL}) \parallel (\bar{Z}_{L2} + \bar{Z}_F) \quad (8)$$

$Z_F$ : Fault impedance.

In three phase fault condition (that is a balance fault.),  $Z_F$  equals to zero approximately and according to Eq. (8),  $|\bar{Z}_{K(F)}|$

will be small. Consequently, comparison of Eq. (2) with Eq. (6) and Eq. (3) with Eq. (7) show that the voltage sag and the phase angle jump occur in the fault interval, respectively. So, the sensitive load experiences worse condition. To prevent voltage sag and phase angle jump during fault, a proper solution is introducing a large limiting impedance between the substation PCC and the fault location. This solution is the base of FCL's operation.

### III. PROPOSED FCL CONFIGURATION AND ITS OPERATION

Fig. 3 shows the circuit topology of the proposed FCL which is composed of two following parts:

1. Bridge part that includes a diode rectifier bridge, a small dc limiting reactor ( $L_{dc}$ ) (Note that, its resistance ( $R_{dc}$ ) is involved, too.), a semiconductor switch (IGBT or GTO), a free wheeling diode ( $D_5$ ).
2. Shunt branch as a compensator that consists of a resistor and an inductor ( $R_{sh} + j\omega L_{sh}$ ).

Previously introduced structures for this application [4, 16, 17], have used two numbers of thyristors at bridge branches instead of one semiconductor switch inside the bridge (dc current route). Therefore, firstly, they have the more complicated control system. Secondly, in those structures, because of thyristors operation delay (turn off at first zero crossing),  $L_{dc}$  has large value to limit the fault current between fault occurrence instant and thyristors turn off instant, properly. This large value of  $L_{dc}$  leads to considerable voltage drop on the FCL and the power losses including ac power losses on the shunt branch impedance and dc reactor power losses (if it is non-superconductor) in the normal condition. By using the semiconductor switch in the proposed structure and its fast operation, it is possible to choose a small value for  $L_{dc}$  to prevent sever  $di/dt$  at the beginning of fault occurrence. So, the voltage drop and power losses will be negligible. Nowadays, high rating semiconductor switches are available in practice. However, using self turn off switch instead of thyristors in the proposed structure leads to more cost [19-21]. From power loss point of view, in the normal condition, the proposed FCL has the losses on the rectifier bridge diodes, the semiconductor switch and  $R_{dc}$ . Each diode of the rectifier bridge is ON in half a cycle, while semiconductor switch is always ON. Therefore, the power losses of this FCL in the normal operation can be calculated as Eq. (9).

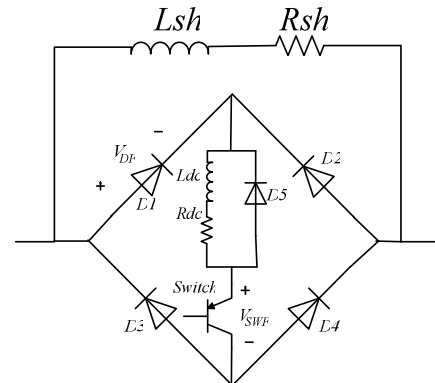


Fig. 3. The proposed FCL topology

$$P_{loss} = P_R + P_D + P_{SW} = R_{dc} I_{dc}^2 + 4V_{DF} I_{ave.} + V_{SWF} I_{dc} \quad (9)$$

where:

$I_{dc}$ : dc side current which is equal to peak of line current ( $I_{peak}$ );

$V_{DF}$ : Forward voltage drop on each diode;

$V_{SWF}$ : Forward voltage drop on the semiconductor switch;

$I_{ave.}$ : Average of diodes current in each cycle that is equal to  $I_{peak} / \pi$ .

Considering Eq. (9) and the small value of dc reactor in this structure, total power losses of the proposed structure becomes a very small percentage of the feeder's transmitted power. For example, by considering Table I parameters in simulation section, the power losses will be 0.47% of the feeder's transmitted power.

On the other hand, in the fault condition, the PCC voltage drops on the shunt impedance. Therefore, the line current will pass through the shunt resistor ( $R_{sh}$ ). As a result, power loss on the  $R_{sh}$  depends on its value that will be discussed in design considerations section. Note that the fault condition is several cycles and it is a small time interval.

#### IV. CONTROL STRATEGY

Fig. 4 shows the control circuit of the proposed FCL. In the normal operation of the power system, the semiconductor switch is ON and the line current ( $i_L$ ) passes through "D1,  $L_{dc}$ , semiconductor switch, D4" and "D3,  $L_{dc}$ , semiconductor switch, D2" in positive and negative alternatives, respectively. So,  $L_{dc}$  is charged to peak of the line current and behaves as a short circuit. Using semiconductor devices (diodes and semiconductor switch) and small dc reactor, cause a negligible voltage drop on the FCL.

When a fault occurs,  $I_{dc}$  become greater than maximum permissible current  $I_m$  and control circuit detects it and turns the semiconductor switch off. So, the bridge retreats from the feeder and the shunt impedance enters to the faulted line and limits the fault current. At this moment, the free wheeling diode discharges  $L_{dc}$ . In fact, the free wheeling diode is used to provide free route for dc reactor current when the semiconductor switch is OFF.

When fault is removed, while semiconductor switch is OFF, shunt impedance will be connected in series with the load impedance. Therefore, line current will be decreased, instantaneously. To detect this instantaneous reduction of line current,  $i_L$  is compared with ( $I_f$ ) that can be calculated from Eq. (10).

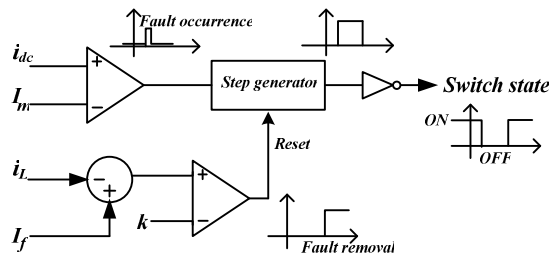


Fig. 4. Control circuit of the proposed FCL

$$I_f = \frac{|\bar{V}_{PCC}|}{|R_{sh} + j\omega L_{sh}|} \quad (10)$$

When the difference of  $i_L$  and  $I_f$  become greater than  $k$  as the fault removal sign, control circuit turns the semiconductor switch ON. So, power system returns to the normal state. The value of  $k$  can be calculated from Eq (11) as follow:

$$k = \frac{|\bar{V}_{PCC}|}{|\bar{Z}_{sh}|} - \frac{|\bar{V}_{PCC}|}{|\bar{Z}_{sh} + \bar{Z}_{L,min}|} \quad (11)$$

where:

$Z_{sh}$ : The shunt impedance;

$Z_{L,min}$ : Minimum impedance of load on the protected feeder.

#### V. DESIGN CONSIDERATIONS

As mentioned previously,  $L_{dc}$  is placed in series with the semiconductor switch to protect it against severe  $di/dt$  at the beginning of fault occurrence. So, its value can be chosen considering current characteristic of the semiconductor switch.

For designing shunt branch parameters, it is possible to consider following conditions. In the ideal case, shunt branch impedance is equal to load impedance. In this condition, when a fault happens in the protected feeder, the voltage sag at the PCC will be zero. However, it is difficult to equate these impedances exactly because of load variation on distribution feeders. So, it is difficult to estimate the best value for  $L_{sh}$  and  $R_{sh}$ . From practical point of view, parameters of shunt branch can be determined by using the history of load measurements at the protected feeder. It is obvious that feeder's power and consequently its current change. For calculation of  $L_{sh}$  and  $R_{sh}$  values, average impedance of the protected feeder is calculated. So,  $L_{sh}$  and  $R_{sh}$  are chosen equal to its inductance and resistance.

From practical point of view, Fig 5(a) and Fig. 5(b) are considered. Fig. 5(a) shows the magnitude of PCC voltage. The horizontal axis of this figure shows the magnitude of load impedance in per-unit where the base value is its impedance of ideal case. The dashed line shows the existence of ideal case. The ratio of reactance to resistance of shunt branch is kept constant in this figure. The parameter of this figure is the magnitude of source impedance. This figure shows that for a wide range of load magnitude variations (0.5 to 2 p.u. with fixed shunt branch impedance), the voltage magnitude of PCC for post-fault condition changes in an acceptable range especially for low values of  $|\bar{Z}_S|$ .

Fig. 5(b) shows the phase angle deviation of the PCC from its base value that is the phase angle deviation of pre-fault PCC voltage. The horizontal axis of this figure is the ratio of reactance to resistance of shunt branch in per-unit where the base value is obtained from ideal condition. This figure shows that it is possible to decrease the resistance of shunt branch (without changing the magnitude of its impedance) in a wide range without any considerable phase angle jump during fault. Decreasing  $R_{sh}$  decreases the power loss of shunt branch during short circuit interval. So, its design becomes simpler.

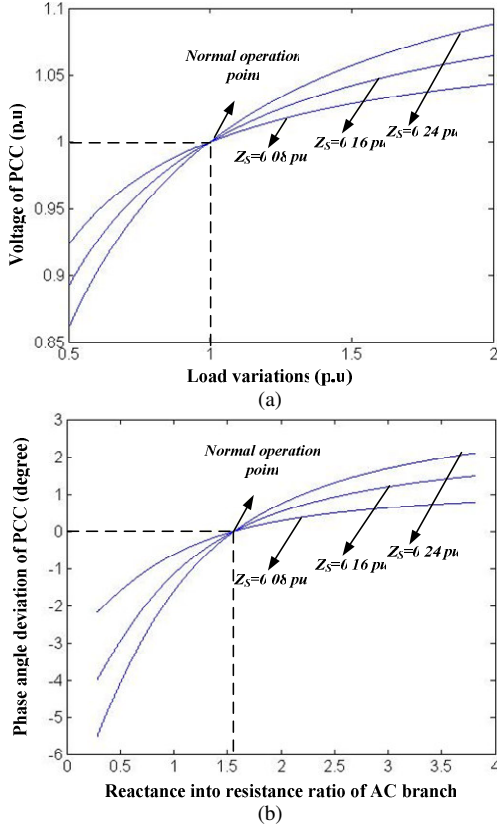


Fig. 5. (a) Voltage magnitude and (b) Phase angle deviation of the PCC when shunt branch impedance is not equal to the protected feeder load impedance (non-ideal case).

## VI. SIMULATION RESULTS AND EFFECT OF THE PROPOSED FCL ON VOLTAGE SAG AND PHASE ANGLE JUMP

With a balanced fault at the F2 in Fig. 1, without using the FCL, the PCC voltage drops, severely. When the FCL is installed in the F2, not only reduces the fault current, but also restores the non-faulted feeder voltage to the normal level. So, the FCL improves the voltage quality and the reliability of the supply network. In this section, analytical analysis of the proposed FCL and simulation results are presented. System parameters are as Table I. These simulations are obtained using the PSCAD/EMTDC software. In addition, considering section IV, to show the practical condition, the values of shunt branch parameters ( $R_{sh}$ ,  $L_{sh}$ ) are the non-ideal case.

Table I. System parameters

Source Side Data	Power source	20kV, 50Hz, X/R ratio: 5 Total Impedance: 1.608 $\Omega$
	Transformer	20 kV/6.6 kV, 10 MVA, 0.1 pu
Distribution feeders data	Feeder F1	j0.314 $\Omega$
	Feeder F2	j0.157 $\Omega$
FCL data	dc side	$L_{dc} = 0.01$ H, $R_{dc} = 0.03$ $\Omega$ $V_{DF} = 3V$ , $V_{SWF} = 3V$ , $I_m = 0.6kA$ Switch type: IGBT
	Shunt branch	$L_{sh} = 0.08$ H, $R_{sh} = 5$ $\Omega$
Load data	Sensitive load	10+ j15.7 $\Omega$
	Load of F2	15+ j31.4 $\Omega$

As shown in Fig. 6, in the fault condition (fault occurs at  $t_0 = 1s$ ), the PCC voltage and power transfer to the sensitive load drop without the FCL. Considering this figure, it shows that zero crossing of the PCC voltage changes before and after fault. With placing the proposed FCL in outset of the F2, when the fault happens, the proposed FCL inserts large impedance into the faulted line and prevents the voltage sag and phase angle jump at the substation PCC. Fig. 7 shows the PCC voltage and sensitive load single phase power in this condition. In the first moments of fault, slight distortion appears in the PCC voltage waveform caused by the semiconductor switch operation and inserting the shunt impedance into the faulted line. After that, the PCC voltage sag and phase angle jump will be in an acceptable range that is discussed in section IV in detail. The power of the sensitive load in this interval has not any considerable change.

In comparison with operation of the structures introduced in [4], [16] and [17], using the semiconductor switch at dc current route in the proposed FCL instead of thyristors at bridge branches, leads to mitigation of sag and distortion in the PCC voltage after fault occurrence (Fig. 8). As shown in simulation results, the proposed FCL can resolve voltage sag and phase angle jump problem properly.

Fig. 9 shows the voltage drop on the proposed FCL during fault. This voltage drop causes that the PCC voltage does not change (considering Fig. 7(a)).

Fig. 10 shows the line current of F2, dc reactor and shunt impedance current ( $i_L(t)$ ,  $i_{dc}(t)$  and  $i_{sh}(t)$  respectively). As shown in Fig. 10(b), between fault occurrence instant ( $t_0$ ) and line current rising to its normal condition's peak instant ( $t_1$ ), the dc reactor current does not change. From instant  $t_1$  to  $t_2$  (semiconductor switch operation instant), the dc reactor charges according to differential Eq. (12).

$$\begin{cases} \omega L_{dc} \frac{di_{dc}(\omega t)}{d\omega t} + R_{dc} i_{dc}(\omega t) + 2V_{DF} + V_{SWF} = V_{PCC} \\ i_{dc}(\omega t = \omega t_1) = I_{peak} \end{cases} \quad (12)$$

where:

$i_{dc}(\omega t)$ : dc reactor current between  $t_1$  to  $t_2$ ;

$V_{PCC} = V_P \sin(\omega t)$ .

Solution of Eq. (13) leads to:

$$i_{dc}(\omega t) = A e^{\frac{-R_{dc}}{\omega L_{dc}} \omega(t-t_1)} + B \sin(\omega t - \varphi_{dc}) + K \quad (13)$$

where:

$$\begin{cases} A = I_{dc} - \frac{V_P}{\sqrt{R_{dc}^2 + \omega^2 L_{dc}^2}} \sin(\omega t_1 - \varphi_{dc}) + \frac{2V_{DF} + V_{SWF}}{R_{dc}} \\ B = \frac{V_P}{\sqrt{R_{dc}^2 + \omega^2 L_{dc}^2}} \\ K = -\frac{2V_{DF} + V_{SWF}}{R_{dc}} \\ \varphi_{dc} = \arctan\left(\frac{\omega L_{dc}}{R_{dc}}\right) \end{cases} \quad (14)$$

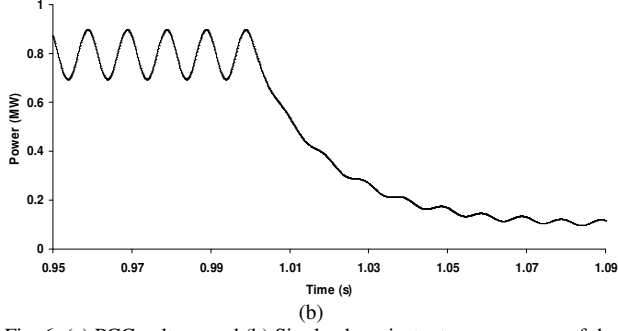
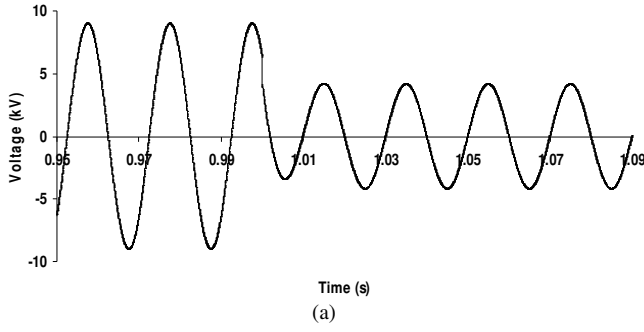


Fig. 6. (a) PCC voltage and (b) Single phase instantaneous power of the sensitive load without FCL

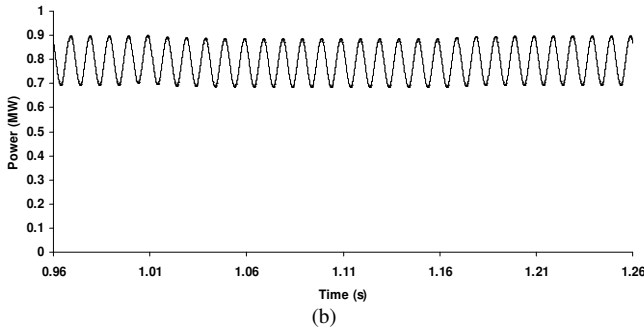
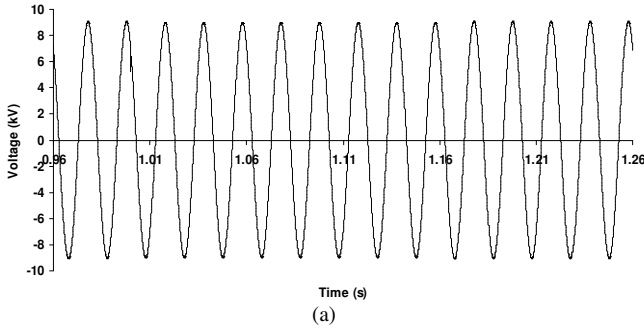


Fig. 7. (a) PCC voltage and (b) Single phase instantaneous power of the sensitive load with the proposed FCL

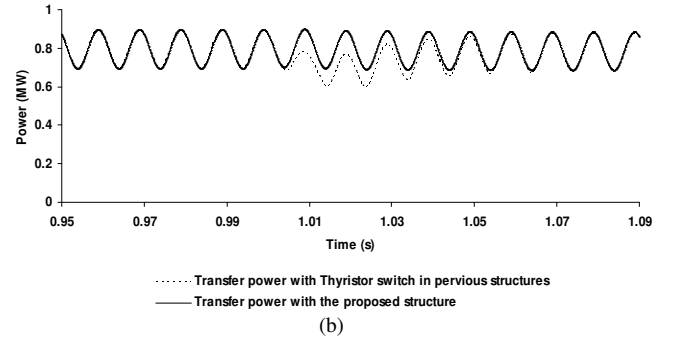
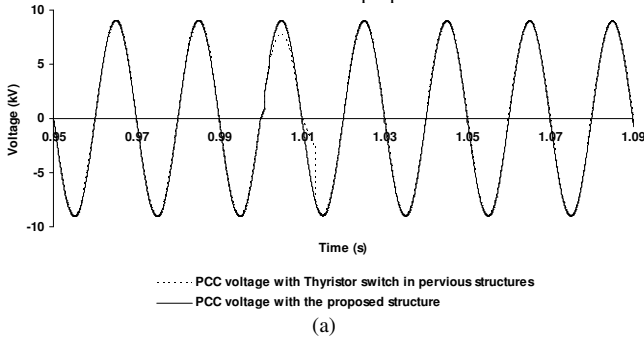


Fig. 8. (a) PCC voltage and (b) Single phase instantaneous power of the sensitive load waveforms with semiconductor switch in the proposed FCL and thyristor switches in previously structures

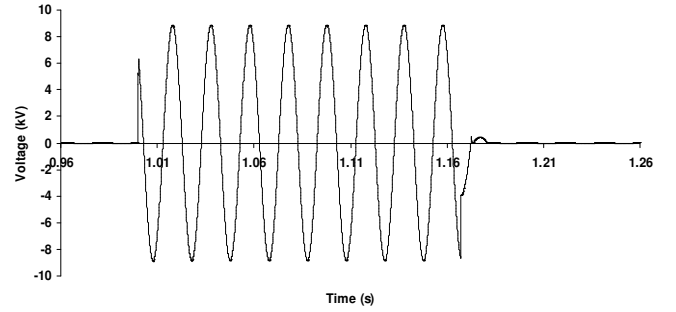


Fig. 9. Voltage drop on the proposed FCL during fault

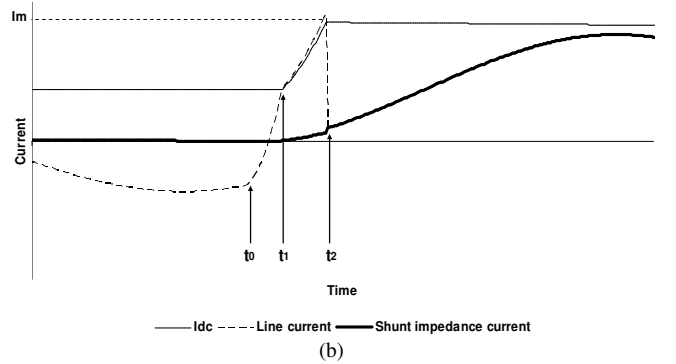
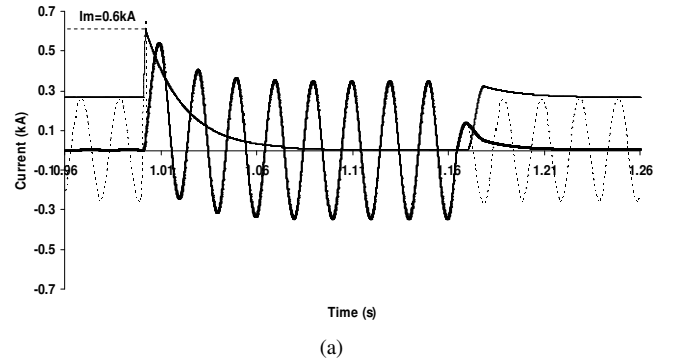


Fig. 10. (a) Line, dc reactor and shunt impedance currents and (b) enlarged view

In addition, at this interval, voltage across the proposed FCL increases shunt impedance current. Differential equation of this current is expressed by Eq. (15):

$$\omega L_{sh} \frac{di_{sh}(\omega t)}{d\omega t} + R_{sh} i_{sh}(\omega t) = V_{PCC} \quad (15)$$

Initial value of  $i_{sh}(\omega t)$  is zero. So:

$$i_{sh}(\omega t) = A e^{\frac{-R_{sh}}{\omega L_{sh}} \omega(t-t_1)} + B \sin(\omega t - \phi_{sh}) \quad (16)$$

where:

$$\begin{cases} A = -\frac{V_P}{\sqrt{R_{sh}^2 + \omega^2 L_{sh}^2}} \sin(\omega t_1 - \phi_{sh}) \\ B = \frac{V_P}{\sqrt{R_{sh}^2 + \omega^2 L_{sh}^2}} \\ \phi_{sh} = \arctan\left(\frac{\omega L_{sh}}{R_{sh}}\right) \end{cases} \quad (17)$$

Note that the time interval between  $t_1$  to  $t_2$  is some milliseconds.

Semiconductor switch control strategy is based on maximum permissible fault current,  $I_m$ . Between  $t_1$  to  $t_2$ , line current ( $i_L(\omega t)$ ) equals to  $i_{dc}(\omega t)$  plus  $i_{sh}(\omega t)$  (Fig. 10(b)). When semiconductor switch current exceeds  $I_m$ , control system of its turns it off. In Eq. (13), if  $i_{dc}(\omega t)$  is equal to  $I_m$ , semiconductor switch operation instant ( $t_2$ ) can be calculated. After  $t_2$ , the diode bridge retreats and the shunt impedance limits the fault current. Until fault clearance instant and turning on the semiconductor switch, the line current follows Eq. (16). In addition, at this interval,  $i_{dc}(\omega t)$  is discharged by  $D_5$  as following equation:

$$\begin{cases} \omega L_{dc} \frac{di_{dc}(\omega t)}{d\omega t} + R_{dc} i_{dc}(\omega t) = 0 \\ i_{dc}(\omega t = \omega t_2) = I_m \end{cases} \quad (18)$$

As a result:

$$i_{dc}(\omega t) = I_m e^{\frac{-R_{dc}}{\omega L_{dc}} \omega(t-t_2)} \quad (19)$$

It is important to note that Eq. (16) is composed of two parts, exponential and sinusoidal. The Exponential part causes a transient in the line current (as shown in Fig. 10(a)) that duration of this transient depends on time constant of the shunt impedance ( $L_{sh}/R_{sh}$ ).

## VII. EXPERIMENTAL SETUP

To show effectiveness of the proposed FCL, an experimental setup is provided and its results are shown in this section. Table II shows parameters of the experimental study.

Fig. 11 shows the PCC voltage in a balanced fault condition by using the proposed FCL. This figure is in agreement with Fig. 7(a). It is obvious that the proposed FCL prevents the voltage sag with negligible distortion only because of semiconductor switch operation. In addition, the phase angle jump on the PCC voltage is mitigated, too

The voltage drop on the FCL is shown in Fig. 12. It is obvious that this figure follows Fig. 9. Fig. 13(a) and 13(b) show the line current of the F2 and the shunt impedance current, respectively. In general, the experimental setup validates the simulation results and shows that the proposed FCL has acceptable capabilities for the voltage quality improvement and the current limiting aims.

Table II. Experimental setup parameters

<b>Source Side Data</b>	Power source	100V peak, 50Hz, 0.5 $\Omega$
	Transformer	100V/100V, 5kVA, 0.1 pu
<b>Distribution feeders data</b>	Feeder F1	j0.2 $\Omega$
	Feeder F2	j0.2 $\Omega$
<b>FCL data</b>	dc side	$L_{dc} = 0.01$ H, $R_{dc} = 0.03$ $\Omega$ $V_{DF} = 1$ V, $I_m = 2.5$ A IGBT: 600V, 40A at $T = 100^\circ$ C, $V_{SW} < 2.5$ V
	Shunt branch	$L_{sh} = 0.1$ H, $R_{sh} = 30$ $\Omega$
	Sensitive load	30+ j47 $\Omega$
<b>Load data</b>	Load of F2	30+ j47 $\Omega$

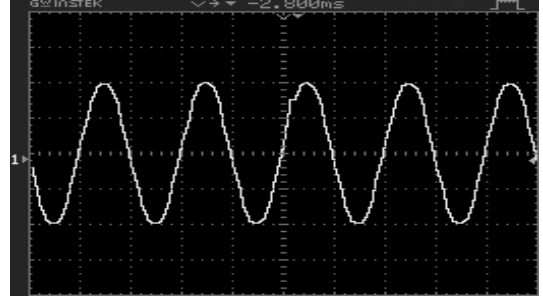


Fig. 11. The PCC voltage with the proposed structure (Volt/div.: 50V, Time/div.: 10ms)

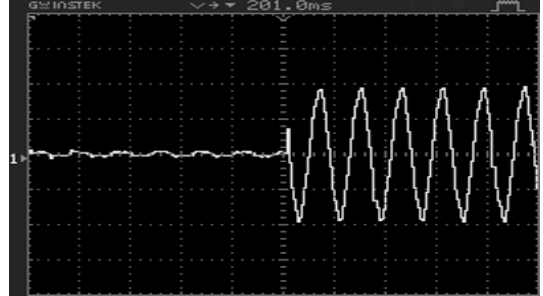
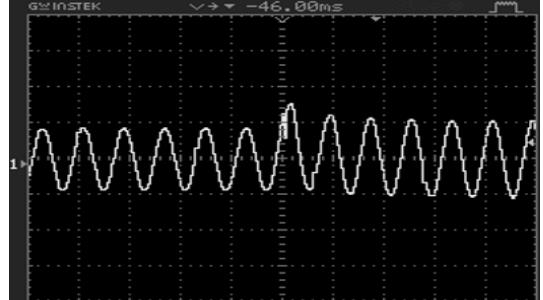
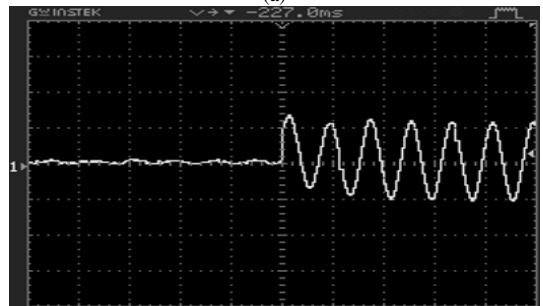


Fig. 12. The voltage drop on the proposed FCL during Fault (Volt/div.: 50V, Time/div.: 25ms)



(a)



(b)

Fig. 13. (a) Line current of the F2, (b) Shunt impedance current (Current/div.: 2A, Time/div.: 25ms)

## VIII. HARMONIC STUDY

As mentioned above, because of using the diodes, the semiconductor switch and the small dc reactor, there is a voltage drop on the FCL. This voltage drop causes harmonic distortion on load voltage and power losses in shunt branch in normal condition.

Using dc voltage source in the proposed structure, Fig. 14, compensates voltage drop on the power electronic devices and the small dc reactor resistance. So, it reduces total harmonic distortion (THD) of voltage waveform [14, 22, and 23]. Its magnitude can be achieved by Eq. (20) as follow:

$$V_{dc} = R_{dc} I_{dc} + 2V_{DF} + V_{SWF} \quad (20)$$

Where,  $V_{SWF}$  and  $V_{DF}$  stand for the voltage drops across the semiconductor switch and each diode, respectively.  $I_{dc}$  is the current of dc route that is equal to the peak of line current in the normal condition. It is important to note that the dc voltage source can be simply provided by a rectifier [14, 15].

Fig. 15 shows load voltage in the normal operation of the power system with and without the dc voltage source and Fig. 16 shows frequency spectrum of the load voltage. By using the dc voltage source, the distortions of voltage waveform decreases to lower values in the normal condition, as shown in Fig. 14 and Fig. 16. THD of the load voltage in case of the proposed FCL without and with the dc voltage source are 2.789% and 0.117%, respectively.

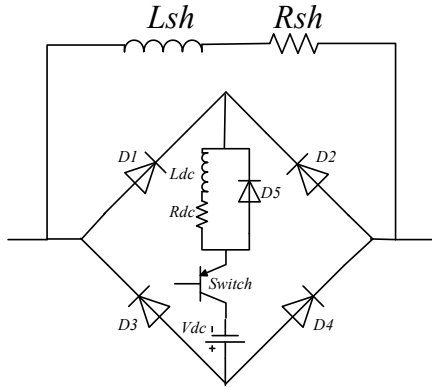


Fig. 14. The proposed FCL topology with dc voltage source

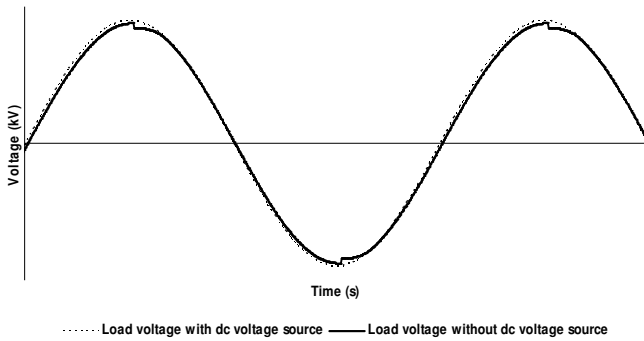


Fig. 15. The load voltage in the normal operation of the power system with and without the dc voltage source

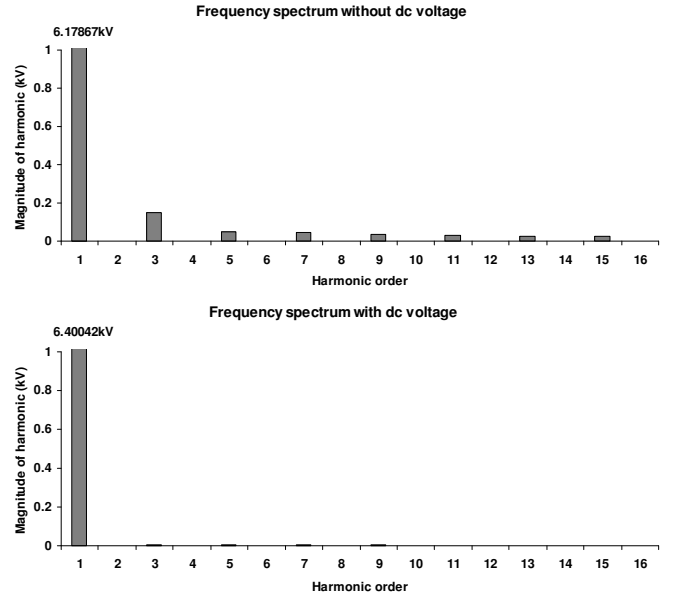


Fig. 16. Frequency spectrum of the load voltage

## IX. CONCLUSION

In this paper, the proposed FCL structure is introduced. Voltage sag compensation, phase angle jump mitigation and fault current limiting operation due to the control method were analyzed. The computer simulation using the PSCAD/EMTDC software and the experimental study are presented to validate results of the analytical analysis. The proposed FCL is capable of mitigating voltage sag and phase angle jump to acceptable levels. Because of using the semiconductor switch in dc current path instead of two numbers of thyristor at the bridge branches, the proposed FCL has high speed and consequently, dc reactor value is reduced to lower value. Note that the control system of this structure is simpler than previous ones. In addition, the dc voltage source placed in the proposed FCL structure reduces its THD and ac losses in the normal operation. In general, this type of FCL with the simple control circuit and low cost is useful for the voltage quality improvement because of voltage sag and phase angle jump mitigating and low harmonic distortion in distribution systems.

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